UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,327	03/24/2004	Takashi Ando	042271	4003

38834 7590 01/28/2008

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
01/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,327	ANDO, TAKASHI	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4,6,8,10,12,13,15,16 and 18-30* is/are pending in the application.

4a) Of the above claim(s) *13,15,16 and 18-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4,6,8,10 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed October 25, 2007.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claim 2 is rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Prior Art.

In regards to claim 2, Applicant's Prior Art discloses the following:

a) a semiconductor substrate (1) (For Example: See Figure 11);

b) a plurality of transistors formed on a surface of said semiconductor substrate (For Example: See Figure 11);

c) an interlayer insulating film (8) for covering said transistors (For Example: See Figure 11);

d) a plurality of ferroelectric capacitors (15) formed over said interlayer insulating film, an electrode of each of said plurality of ferroelectric capacitors being connected to one of a source or a drain (6) of said transistors via a first contact plug (9),wherein said plurality of ferroelectric capacitors are arranged in an array extending in longitudinal and lateral directions, (For Example: See Figure 11);

e) a plurality of bit lines (11) formed over said interlayer insulating film, each of said plurality of bit lines being connected to other of the source or the drain of said transistors via a second contact plug (10) (For Example: See Figure 11); and

f) wherein the second contact plug is located in a region including an intersection of two diagonal lines in said four closest ferroelectric capacitors out of said plurality of ferroelectric capacitors (For Example: See Figure 10).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art.

In regards to claim 4, Applicant's Prior Art fails to disclose the following:

a) a straight line connecting the source and the drain of said transistors extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors.

However, the Applicant has not established the critical nature of "a straight line connecting the source and the drain of said transistor extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

6. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Summerfelt et al. (U.S. Publication No. 2005/0012125).

In regards to claim 6, Applicant's Prior Art fails to disclose the following:

a) an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors, and wherein a first straight line connecting a first source and a first drain of one of said two transistors substantially coincides with the second straight line connecting a second source and a second drain of second one of said two transistors.

However, Summerfelt discloses a semiconductor device that has an element isolation insulating film (8) formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors, and wherein the line connecting the source and the drain of one of said two transistors substantially coincides with the line connecting the source and the drain of the other one of said two transistor (For Example: See Figure 1A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors, and wherein the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor as disclosed in Summerfelt because it aids in separating the transistors source/drains (For Example: See Paragraph 29).

Additionally, since Applicant's Prior Art and Summerfelt are both from the same field of endeavor, the purpose disclosed by Summerfelt would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 10, Applicant's Prior Art fails to disclose the following:

a) the other of the source or the drain of said transistors is shared by said two transistors in each element region.

However, Summerfelt discloses a semiconductor device that has the other one of the source or the drain of said transistor is shared by said two transistors in each element region (For Example: See Figure 1A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has the other one of the source or the drain of said transistor is shared by said two transistors in each element region as disclosed in Summerfelt because it aids in reducing the capacitance (For Example: See Paragraphs 7 and 8).

Additionally, since Applicant's Prior Art and Summerfelt are both from the same field of endeavor, the purpose disclosed by Summerfelt would have been recognized in the pertinent art of Applicant's Prior Art.

7. Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Summerfelt et al. (U.S. Publication No. 2005/0012125) and Corvasce et al. (U.S. Patent No. 6,656,801).

In regards to claim 8, Applicant's Prior Art fails to disclose the following:

a) an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors.

However, Summerfelt discloses a semiconductor device that has an element isolation insulating film (8) formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors (For Example: See Figure 1A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors as disclosed in Summerfelt because it aids in separating the transistors source/drains (For Example: See Paragraph 29).

Additionally, since Applicant's Prior Art and Summerfelt are both from the same field of endeavor, the purpose disclosed by Summerfelt would have been recognized in the pertinent art of Applicant's Prior Art.

b) a first straight line connecting a first source and a first drain of one of said two transistors is substantially orthogonal to a second line connecting a second source and a second drain of the other one of said two transistor.

However, Corvasce discloses a semiconductor device that has the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor (For Example: See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other

one of said two transistor as disclosed in Corvasce because it aids in providing minimal cell size (For Example: See Abstract).

Additionally, since Applicant's Prior Art and Corvasce are both from the same field of endeavor, the purpose disclosed by Corvasce would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 12, Applicant's Prior Art fails to disclose the following:

a) the other one of the source or the drain of said transistors is shared by said two transistors in each element region.

However, Summerfelt discloses a semiconductor device that has the other one of the source or the drain of said transistor is shared by said two transistors in each element region (For Example: See Figure 1A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has the other one of the source or the drain of said transistor is shared by said two transistors in each element region as disclosed in Summerfelt because it aids in reducing the capacitance (For Example: See Paragraphs 7 and 8).

Additionally, since Applicant's Prior Art and Summerfelt are both from the same field of endeavor, the purpose disclosed by Summerfelt would have been recognized in the pertinent art of Applicant's Prior Art.

Response to Arguments

8. Applicant's arguments filed 10/25/07 have been fully considered but they are not persuasive. Applicant argues that the prior art fails to disclose "wherein the second contact plug is located in a region including an intersection of two diagonal lines in said four closest

ferroelectric capacitors out of said plurality of ferroelectric capacitors." However, Applicant's Prior Art discloses "wherein the second contact plug is located in a region including an intersection of two diagonal lines in said four closest ferroelectric capacitors out of said plurality of ferroelectric capacitors" (For Example: See Figure 10).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization

where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

ML

January 20, 2008

MONICA LEWIS
PRIMARY PATENT EXAMINER